Total Charge Measurement and Control

Edward Herbert
Canton, CT 06019

Revised April 18, 2006

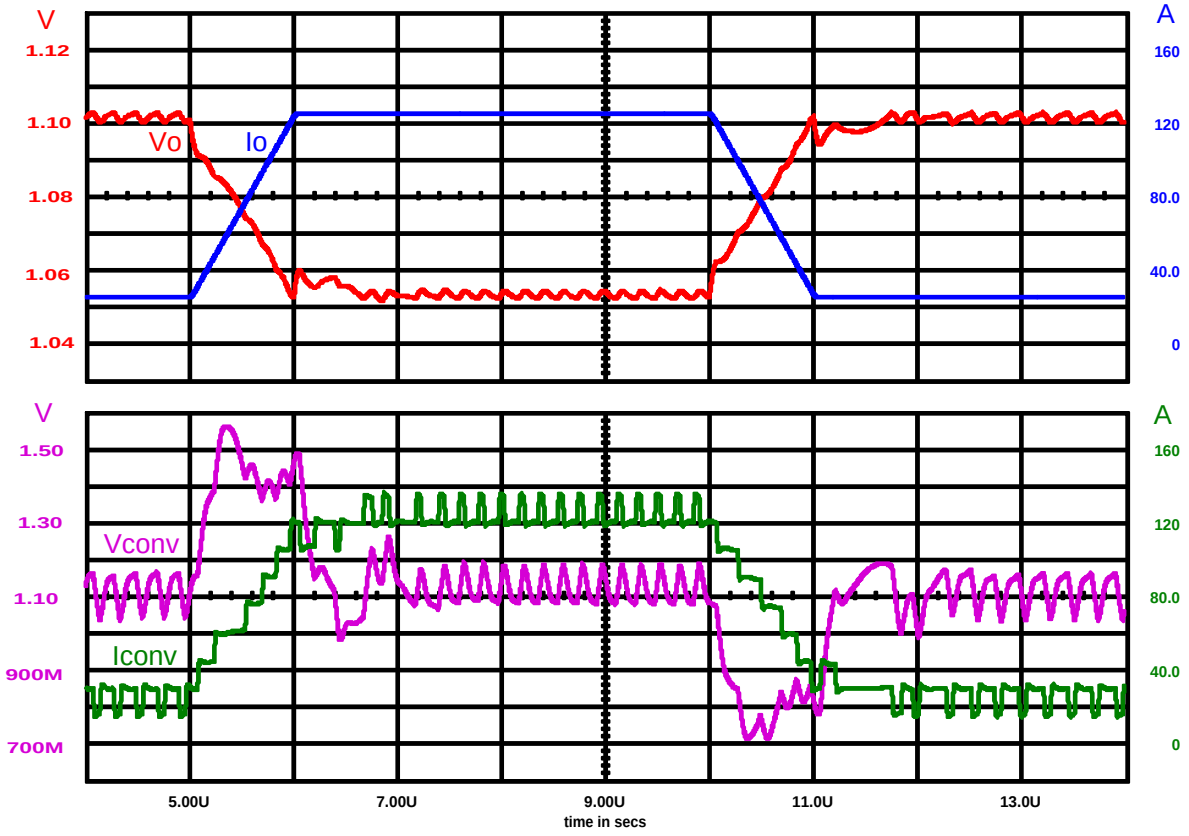
Total Charge Measurement and Control

Abstract:

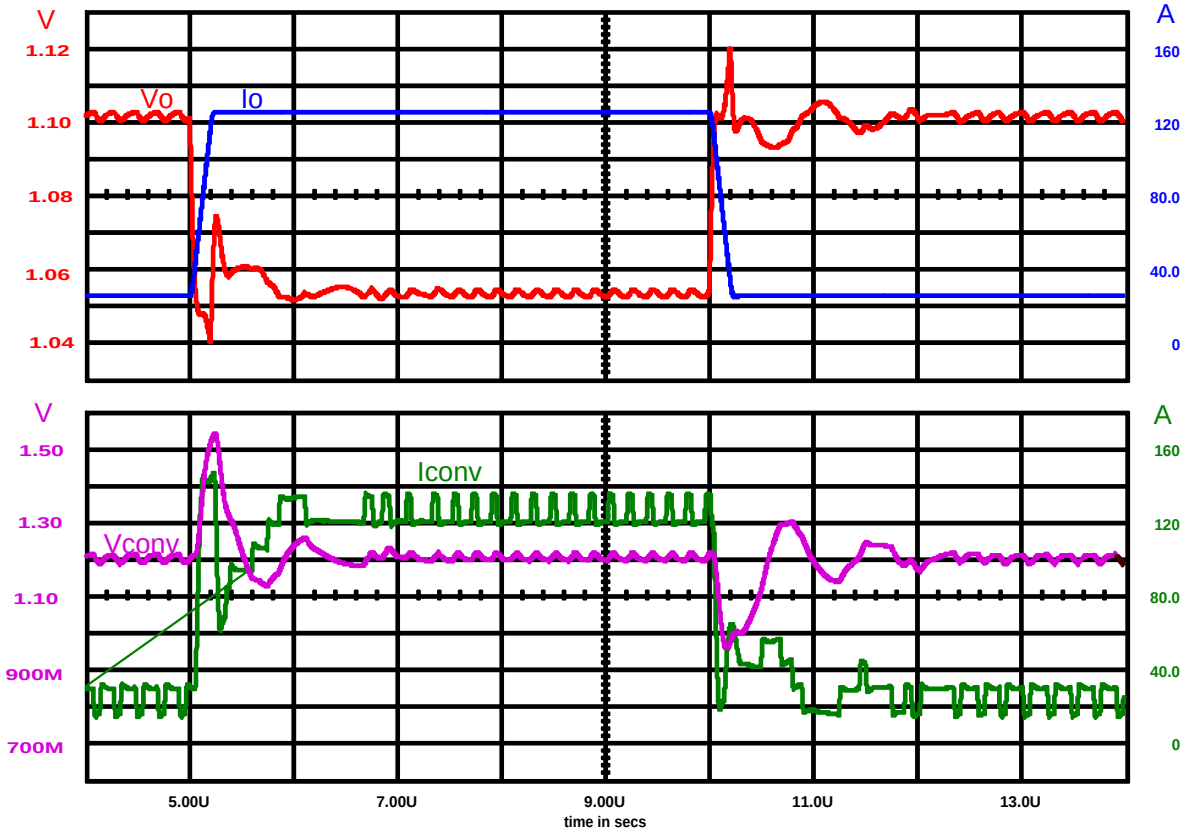
A very fast power converter needs a very fast measurement and control. The remotely sensed output voltage Vo of a power converter is not a suitable control input, as it takes too long to settle. The output current is even worse, and measuring it is horribly complicated. The solution is to measure the total charge on the distributed capacitors in the power train. It is very simple, very fast and unconditionally stable. With total charge control, a very well controlled high driving voltage overcomes the impedance of the motherboard and socket, allowing very fast di/dt with no overshoot and a 1 us settling time, for both rapid increases in load and load dump.

By controlling the total charge on the distributed capacitors of the power converter and motherboard, the impedance of the current path is effectively attenuated by the ratio of the power converter output decoupling capacitors to the total capacitance, a factor of 1/65 in an example shown below.

Transient, 100 A/us



Transient, 500 A/us



Total Charge Measurement and Control

1.0 Total Charge Measurement and Current Control for a Switched Charge Power Converter:

A new voltage and current control scheme for the switched current power converter (SCPC) is based upon measurement of the total charge using a flash analog to digital converter, with the outputs of the flash d-a converter directly controlling the switches of the current sources. For more information on the switched current power converter, please see Switched Current Power Converters at http://eherbert.com. The theory of operation for the total charge measurement is shown later in this presentation.

A power converter, such as the SCPC, that can go from 0 V and 0 A to any VID voltage and full output current in 2 us, and that can respond to load changes or step changes in voltage in tens of nanoseconds requires a very fast and stable measurement and control circuit. Usual feedback circuits with their lags and compensation networks cannot be used. The current must be controlled precisely, yet current measurement cannot be used for the control, as it is much too slow. Voltage measurement is problematical as well, if the circuit has any parasitic inductance, as it can take a long time for the output voltage to settle down and be stable, far too long for use in a fast control.

Measurement of the total charge on the distributed output capacitors provides an elegant solution. It is very fast and unconditionally stable.

The graphs on the page 3 show SPICE simulations of the response to 100 A step changes of the load current through a representative motherboard and socket model, with rates of change of 100 A/us and 500 A/us. Note that the switched current power converter maintains control of the output voltage through the transients.

The first graph shows the output current stepping up then down 100 A in 1 us and the simulated voltage on the processor socket. The graph immediately underneath shows the switched current power converter output voltage and current. The SCPC maintains regulation throughout the transients, and there is no overshoot in either direction.

The third and fourth graphs show a transient of 100 A in 0.2 us, or 500 A/us. There is a small overshoot, but the voltage is stable within 1 us.

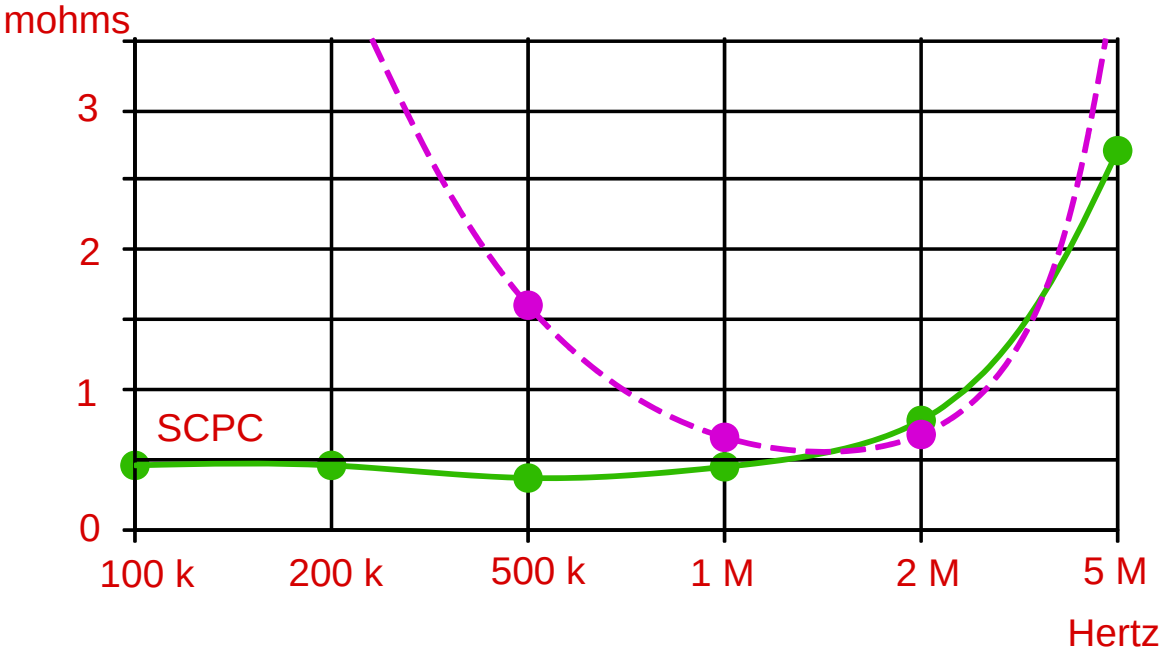
The graph on page 5 shows the simulated large signal impedance at the processor socket for the SCPC, as well as a redacted schematic (the SPICE model used for the motherboard and socket is proprietary). The large signal output impedance model uses a simulated load of 60 A with a superimposed sine wave of 50 A_{p-p}. The output voltage ripple V_{p-p} is measured, and the impedance at each frequency is calculated as $V_{p-p}/50$.

The dashed line is the passive output impedance, derived by running the same test with a static 60 A input. Above 2 MHz, the power converter no longer controls the impedance.

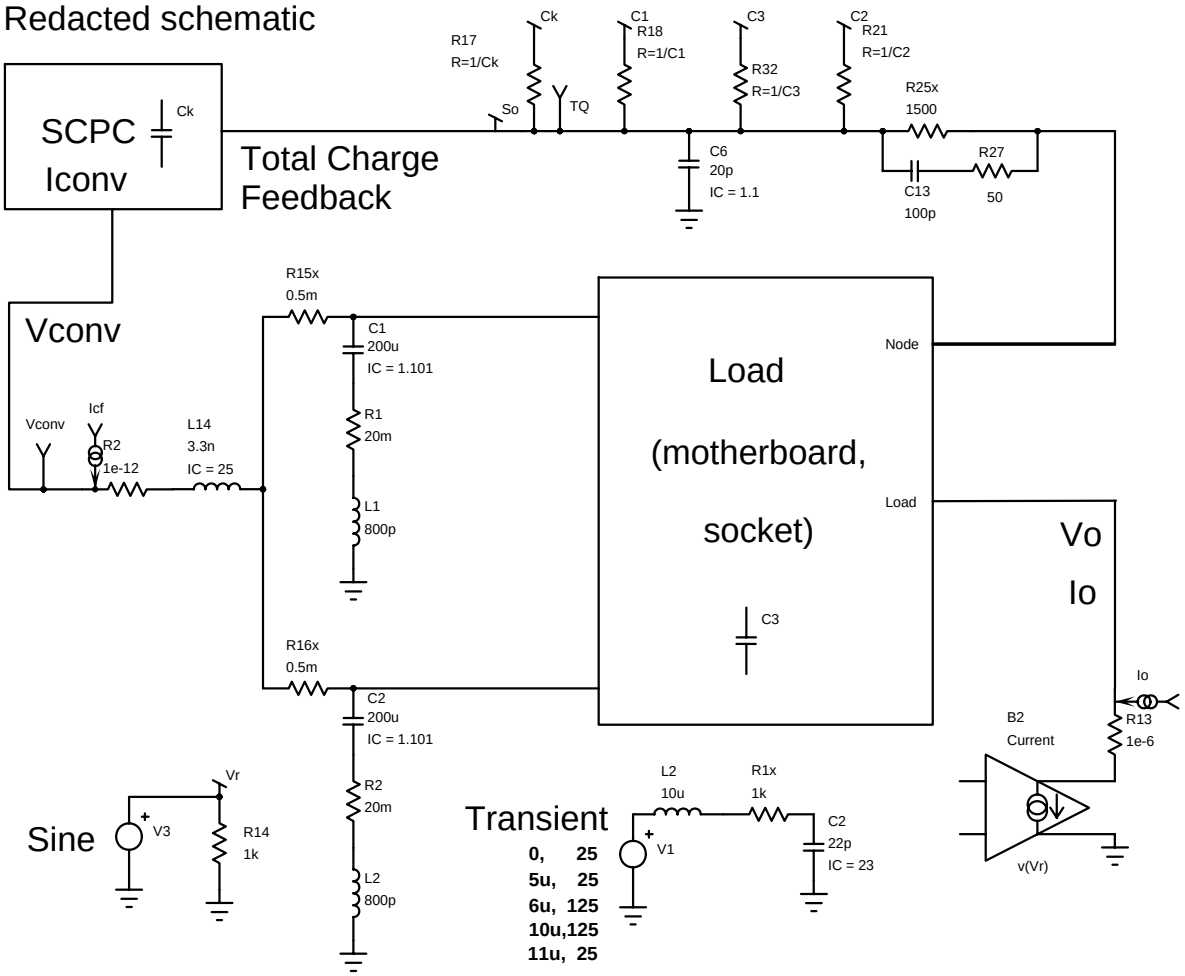
The schematic diagram shows that the bulk capacitors, at 400 uF total, are greatly reduced, compared the bulk capacitors needed for a multi-phase buck-derived VRD.

Switched Current Power Converter

Impedance vs Frequency



Redacted schematic



Total Charge Measurement and Control

1.1 Principle of operation:

The total charge measurement is easily understood with reference to the equation for charge Q on a capacitor C, give a voltage V:

$$Q = C V$$

where charge is in coulombs, the capacitance is in farads and the voltage is in volts.

The simplified schematic on page 7 shows a power converter that is a controlled current source providing current to a microprocessor through an impedance Z. The output capacitor of the power converter is 10 uF, and the capacitors associated with the microprocessor are 650 uF, for a total capacitance of 660 uF.

At a time t_0, both capacitors are at 1 V, with charges of 10 uC and 650 uC, respectfully, so the total charge is 660 uC.

At a time t_1, the load current has increased, removing some charge from the microprocessor capacitor, and reducing the output voltage to 0.995 V. The charge on the microprocessor capacitor is reduced to 646.75 uC.

Initially, the impedance Z blocks any immediate current flow. To maintain the required total charge of 660 uC for the circuit as a whole, the converter current Ic increases sufficiently so that the charge on the first capacitor increases to 13.25 uC, which causes its voltage to rise to 1.325 V. This provides a difference voltage of 0.330 V across the impedance Z, resulting in a very rapid but controlled flow of current.

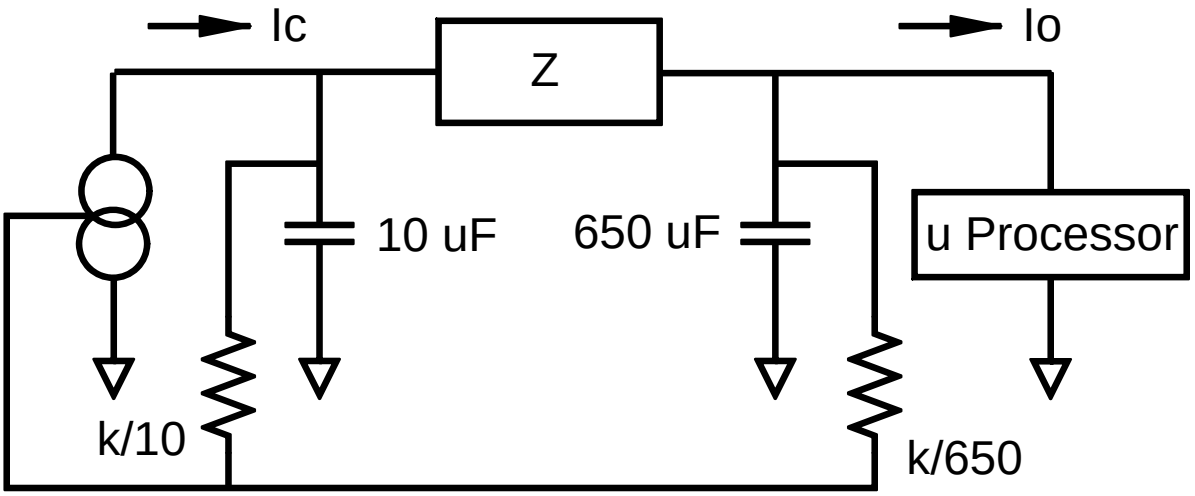
The charge then flows to the microprocessor capacitor. As the charge leaves the converter output capacitor, the voltage settles down, but the total charge of 660 uC is always maintained.

By maintaining the total charge at a constant value, the converter current Ic necessarily equals the output current Io (remember that current is the flow of charge, and amperes equals coulombs per second).

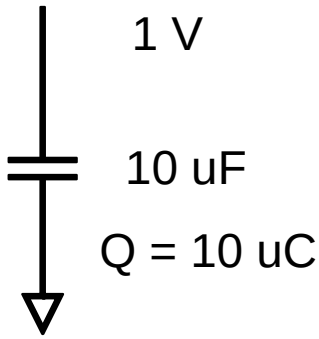
The total charge measurement is made by sampling the voltages of the various capacitors with summing resistor that are inversely proportional to the respective capacitances, k/Cn, as shown in the first figure on page 7.

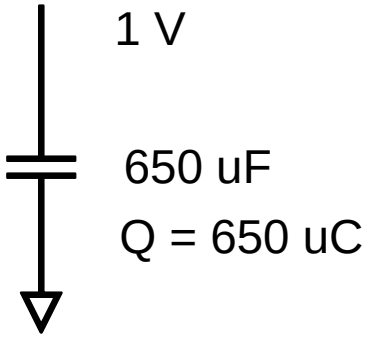
1.1.1 SPICE model:

One identifiable lag in the switched current power converter is the propagation delay through the comparators and the logic, and the switching times of the MOSFETs. In the SPICE simulations of page 3, and for the impedance curve of page 5, the SPICE model included a delay of 50 ns for turn on and 35 ns for turn off.



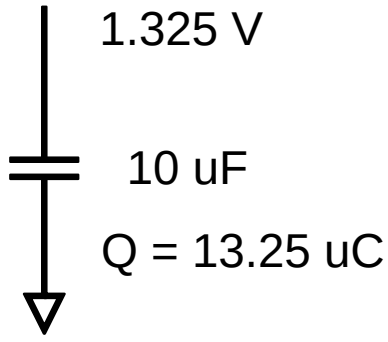
t0

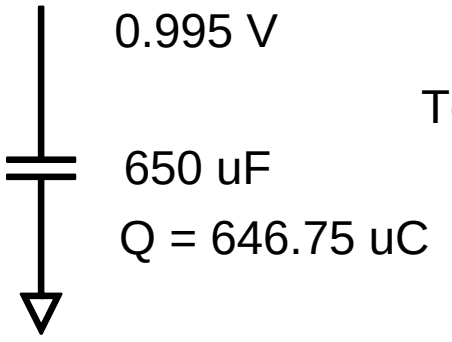




Total Q = 660 uC

t1





Total Q = 660 uC

dV = 0.330 V

Total Charge Measurement and Control

2.1. "Total Charge" Measurement and Control:

The most important function of a control circuit for a power converter is to adjust the converter current so that it equals the output current. This is a necessary condition at steady state. Once current equilibrium is achieved, the converter current may then be adjusted somewhat, up or down, to correct errors in the voltage. Conceptually, the output current could be measured and the converter current could be adjusted to match. Unfortunately, measuring the output current is not useful as a control input, because it is much too slow and the circuits required to measure the current are very cumbersome.

2.1.1. Capacitor Charge as a Control Function:

Current, in amperes, is the flow of charge, in coulombs per second. The voltage on a capacitor is the charge stored in the capacitor times the capacitance. If the current into a capacitor does not equal the current out of the capacitor, the stored charge changes and so does the capacitor voltage. Thus change in the capacitor voltage is an easy and very fast way to determine that there is an error in the converter current.

2.1.2 Parasitic Impedances:

In a practical power converter for a processor, the power delivery system will have parasitic impedances. Of particular concern are the series parasitic inductances, because they cause a system using direct feedback of the output voltage Vo to become unstable. This is because the voltage on the output capacitor does not immediately change in response to an increase in power converter current. The upstream capacitors, on the input side of the parasitic inductance, can store significant excess charge before any of the charge (current) flows to the output capacitor. Thus there is a lag in the output voltage Vo. While the circuit can be compensated, the compensation slows down the circuit response to transients and a very much larger output capacitor is needed.

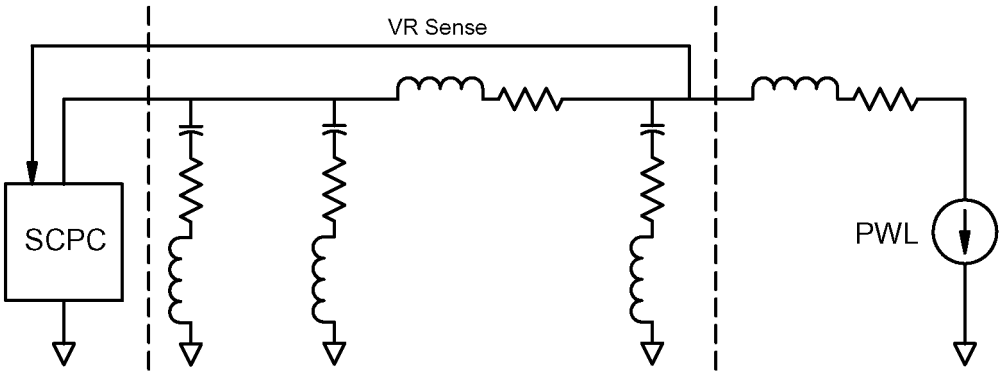


Figure 2.1.1. With series inductance, even a small parasitic inductance, the direct control of the converter current as a function of the output voltage becomes unstable, and large oscillations build very rapidly. While the circuit can be compensated, the compensation slows down the circuit response to transients and a very much larger output capacitor is needed.

2.1.3. Total Charge Sensing Improves Stability and Response:

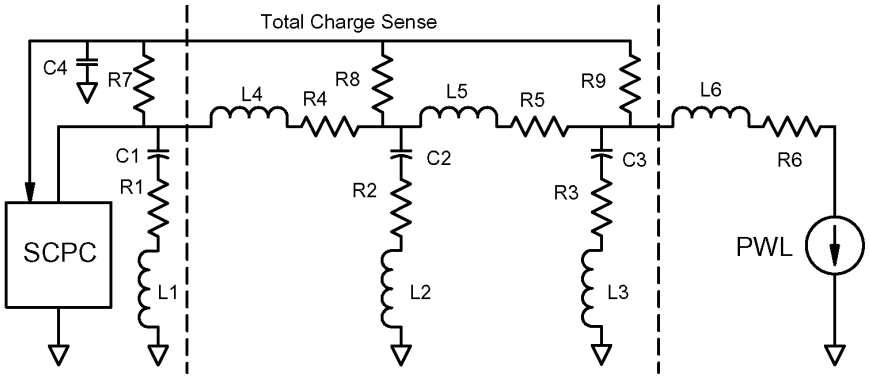


Figure 2.1.2. Total charge sensing can be substituted for output voltage sensing, and it is unconditionally stable. The response need not be compromised by a compensation network, but the series parasitic resistance does affect the output voltage slightly.

This problem of instability due to the parasitic inductances is overcome if the charges on all of the capacitors in the power converter are measured and summed as the control input. Once again the circuit is exquisitely sensitive to differences between the converter current and the output current. The converter current is precisely controlled, the bandwidth is very high (greater than 5 MHz) and it is unconditionally stable.

If the power distribution system is under-damped, there may be oscillations and ringing in the voltages on the various capacitors, but this is invisible to the control system. In SPICE simulations, using representative parasitic impedances from Intel® VR10.2, it seems that a typical layout is fairly well damped, but this is an area of concern for designers.

2.1.4. Total Charge Measurement, ΣQ (Theory):

If the total charge in the various capacitors is measured and summed, a much faster and more accurate control is possible. To introduce the concept of total charge, ΣQ, please see figure 2.1.3, which implements the voltage measurement of figure 2.1.2, except that differential measurement is used to account for ground differences.

The voltages of the various capacitors C1 through C3 are measured, preferably differentially to account for ground differences. The charge on a capacitor is determined as the voltage times its capacitance. If the summing resistors R1 through R3 have their *conductivity* (1/R) proportional to the capacitance, the output of the summing amplifier is proportional to the total charge, ΣQ. Because the total charge ΣQ is linearly proportional to the voltage, it can be used for control purposes as a substitute for the output voltage, with appropriate scaling. $\Sigma Q = \Sigma(Vn\ Cn)$ (the total capacitance ΣCn is assumed to be constant).

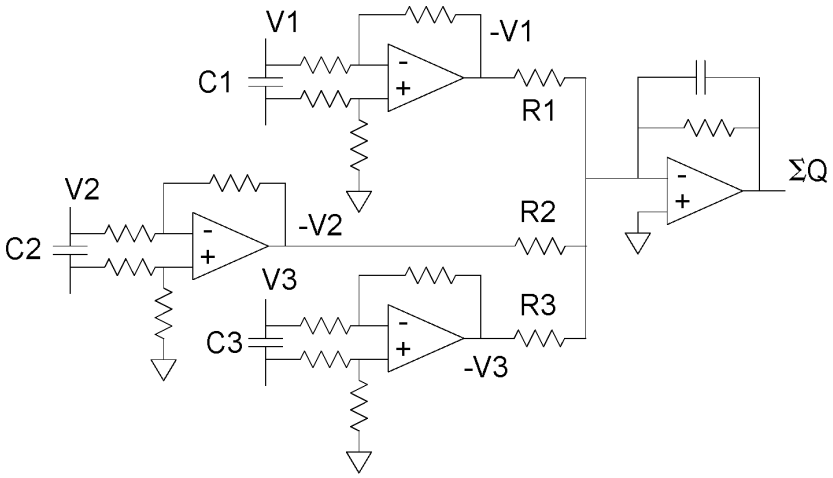


Figure 2.1.3. The voltages of the various capacitors in the system are measured differentially, to remove ground differences. The voltages can then be summed, factored by the value of each capacitor. The sum is the total charge, ΣQ.

2.1.5. Simpler, Faster Charge Measurement:

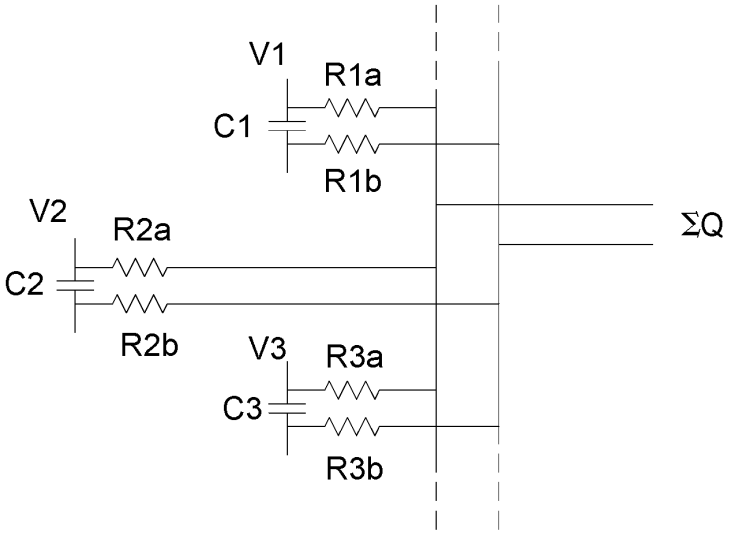


Figure 2.1.4. If the *conductivity* (1/R) of the resistors is proportional to the capacitance of the associated capacitors, the output is proportional to the total charge, ΣQ.

The circuit of figure 2.1.3 is useful for explaining the concept of total charge measurement, but it has the disadvantage that a large number of precision resistors and very fast amplifiers are needed, especially if a large number of points in the circuit are to be measured. Further, the settling time through the amplifiers in series, each with its response and slew rate limitations, results in a significant lag. A much simpler and faster circuit is shown in figure 2.1.4.

Total Charge Measurement and Control

Measurement points consisting of two resistors can connect the various capacitors throughout the power distribution to the total charge measuring system, as shown, one on the power side and one on the return side at each capacitor (or group of capacitors). Three resistor pairs are shown in figure 2.1.4, for simplicity, but it is contemplated that a number of measurement points would be used, including the existing voltage sense pins on the processor package. The resistors need not be precise. Likely, screened on resistive ink would suffice.

The relationship of the resistors can be expressed by the following equations:

$$C1\ R1a = C2\ R2a = C3\ R3a = \text{-----} = Cn\ Rna$$
$$C1\ R1b = C2\ R2b = C3\ R3b = \text{-----} = Cn\ Rnb$$

There may be transmission line effects, and it may be advantageous to consider impedance matching in choosing the value of the resistors, particularly the ones that are furthest from the control circuits. Obviously, they cannot all be the ideal value for impedance matching, but the more critical resistors can be optimized, and the others can be selected as ratios of them using the above formulae.

Note that the equations do not require that the high side resistors and the low side resistors be equal, and it may be desirable to use smaller resistors in the return side, for a lower impedance ground return. Such considerations are a tradeoff of a particular application.

2.1.6. Calculating the Output Voltage, Vo:

Control of the total charge ΣQ does not control the output voltage Vo directly, unless the output voltage Vo is taken directly from the capacitor and there is only one capacitor (or there is zero impedance between capacitors). With distributed capacitors having parasitic impedance between them there will be voltage drops in the system, which will affect the output voltage Vo. At steady state conditions, only the resistances are applicable, and the output voltage calculations are straightforward. For transient conditions, it is suggested that a SPICE simulation be used with all identifiable parasitic impedances included.

If the stray inductances are removed, the schematic of figure 2.1.2 reduces to the schematic of figure 2.1.5. This is valid for steady state conditions, and is used to calculate the "error" introduced by using total charge instead of Vo as the control input.

Total Charge Measurement and Control

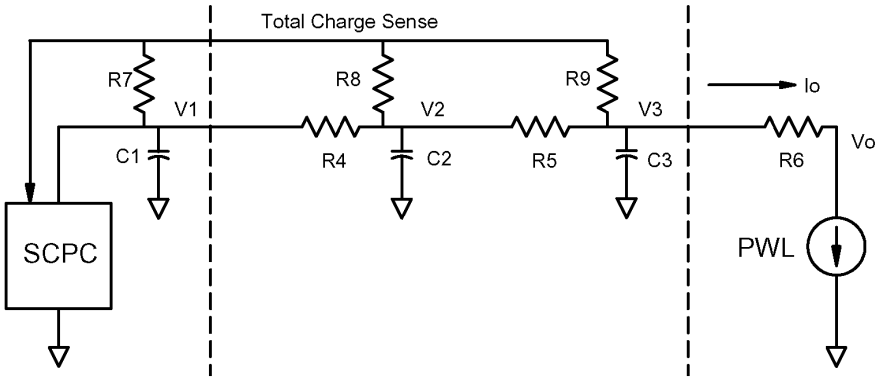


Figure 2.1.5. For steady state conditions, the circuit of figure 2.1.2 reduces to this equivalent circuit. Because R7, R8 and R9 are large, they conduct negligible current, so the average current from the SCPC equals the output current.

To calculate the output voltage Vo at steady state conditions (with reference to figure 2.1.5), let V1, V2 and V3 equal, respectively, the voltages on the capacitors C1, C2 and C3.

By inspection, the charge on the three capacitors is

$$Q1 = C1\ V1$$
$$Q2 = C2\ V2$$
$$Q3 = C3\ V3.$$

Therefore, the total charge ΣQ is given by

$$\Sigma Q = C1\ V1 + C2\ V2 + C3\ V3$$

Also, by inspection, given an output current Io,

$$V1 = Vo + Io\ (R4 + R5 + R6)$$
$$V2 = Vo + Io\ (R5 + R6)$$
$$V3 + Vo + Io\ R6$$

To simplify the final expression, let us define a total capacitance ΣC, a total charge reference ΣQR, and an equivalent resistance RE as follows:

$$\Sigma C = C1 + C2 + C3, \text{ in farads}$$
$$\Sigma QR = \Sigma Q / \Sigma C, \text{ in volts}$$
$$RE = (C1/\Sigma C)\ R4 + ((C1 + C2)/\Sigma C)\ R5 + R6, \text{ in ohms}$$

Substituting, collecting terms and rearranging yields the following expression for the output voltage Vo:

$$Vo = \Sigma QR - Io\ RE$$

It can therefore be seen that ΣQR equals the no load output Voltage, Vo0, and RE is a resistive impedance term. It can be seen that if C1 and C2 are small compared to the total capacitance ΣC, then RE is dominated by R6.

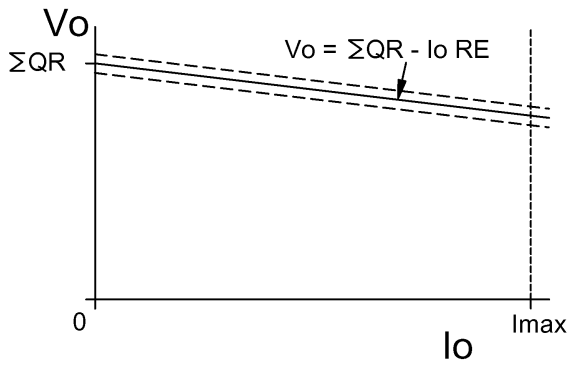


Figure 2.1.6. The output voltage Vo as a function of the output current Io using total charge ΣQ control.

2.1.6. Output Voltage Vo for a SCPC Using Total Charge Control:

When total charge control ΣQ is used with a switched current power converter that uses a flash a-d to directly control the current switches, the total circuit impedance is the sum of the impedance Rs due to the resistor ladder network of the flash a-d converter plus the impedance RE due to the total charge ΣQ control.

$$Vo = Vo0 - Io\,(Rs + RE)$$

For more information on the switched current power converter, please see Switched Current Power Converters at http://eherbert.com.

Improved layout and components can improve the parasitic impedance RE.

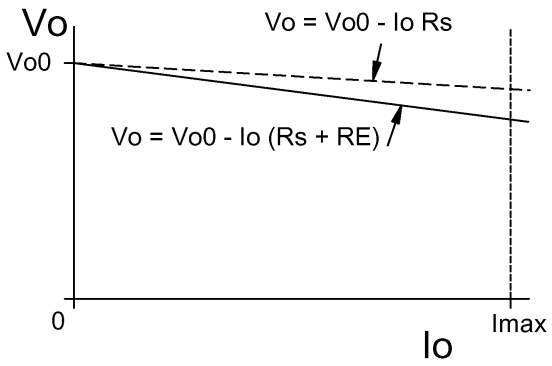


Figure 2.1.7. When total charge ΣQ control is used with a switched current power converter in which a flash a-d directly controls the current switches, Rs and RE combine to define the total circuit impedance.

2.1.7. Overcoming Parasitic Impedance.

A serious impediment to using a plug-in VRM is the problem of the connector's parasitic impedance, particularly the parasitic inductance. The total charge control overcomes the effects of this parasitic impedance, making it less important as a design tradeoff.

For a low voltage, high current power supply of conventional design, parasitic impedances in the path of current flow is a serious problem. It takes a significant driving voltage to increase the rate of current flow in an inductor, and a higher driving voltage just is not available with present VRMs. This problem is overcome with a SCPC using total charge measurement and control.

The equations from 2.1.6, repeated below, show that the impedance R4 is significantly attenuated if C1 is small compared to the total capacitance, ΣC. In the circuit of figure 2.1.5, the impedance R4 simulates an impedance at the connector of a remote VRM. The decoupling capacitors are assumed to be on the motherboard near the processor.

$$RE = (C1/\Sigma C) R4 + ((C1 + C2)/\Sigma C) R5 + R6, \text{ in } \Omega$$

$$Vo = \Sigma QR – Io\ RE$$

An expression in an equation makes more sense with a feel for what is happening in the circuit, empirically. The capacitor C1 may be, as an example, the output capacitor of a VRM that is remote from the MLCC capacitors and the processor. However, it is part of the total charge sensing circuit, and, being directly connected to the VRM, it will be the first to see a response to a drop in the output voltage and the total charge. As an example, let us consider a two capacitor system where the VRM decoupling capacitor C1 is 20 μF, and the output capacitance C3 is 380 μF, for a total capacitance ΣC of 400 μF. If the output voltage decreases 5 mV, the total charge Q is decreased by 2 μC. If this charge is replaced initially entirely on C1, it will result in a voltage rise of 100 mV. This is sufficient voltage to drive the current through the parasitic impedance. Yet the total charge sensing and control prevents the voltage from rising excessively. As the charge is transferred to the output capacitor C3, the voltage on the input capacitor C1 decreases so that the total charge ΣQ remains correct.

The total charge system measures total charge ΣQ, and it is immune to voltage oscillations within the power distribution network. It will maintain the correct total charge ΣQ even if the voltages at the various capacitors are ringing. It is very desirable that the power distribution be a damped system. Because the imaginary part of the complex inductance is lossy, and the losses increase rapidly with frequency, it is likely that most real power distribution systems will be damped at the critical frequency.

Total Charge Measurement and Control

2.1.8. Modified Total Charge Sensing

Performance may be improved with the addition of a resistor from the total charge sense to the output voltage Vo, as shown by R3 in figure 2.1.8. (In the SPICE models, a lead-lag network is used here, resulting in a lower output impedance to a higher frequency).

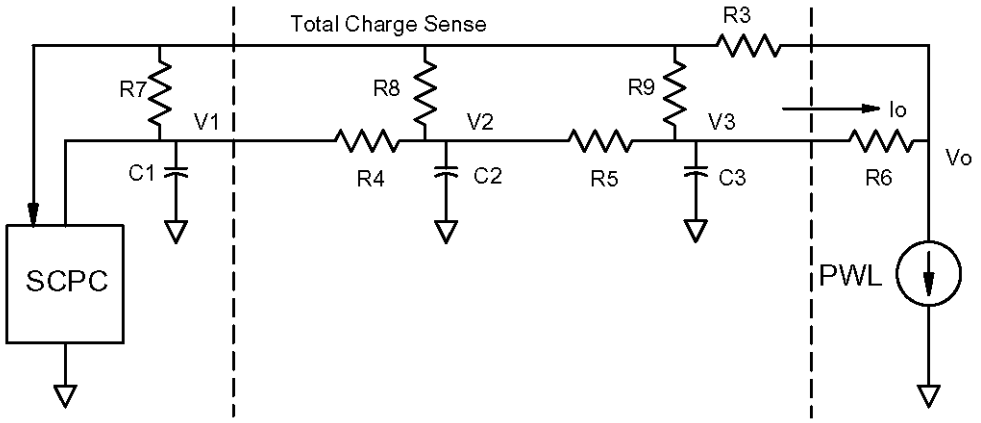


Figure 2.1.8. The total charge sense can be modified with a resistor to the output voltage. In the SPICE models, a lead-lag network was used for R3.

Let us define a resistance Rp equal to the parallel combination of R7, R8, and R9. Using R3, the equation of 2.1.7 ($Vo = \Sigma QR - Io\ RE$) becomes

$$Vo = \Sigma QR - Io * RE\left(\frac{R3}{R3 + Rp}\right)$$

In the SPICE models, R3 is approximately equal to Rp and has a lead-lag around it. The impedance attributable to the total charge sense is reduced by one half and the response at 5 MHz is significantly improved. In the limit, with a very small R3, the circuit reduces to a feedback from Vo, and stability issues will be seen as the benefits of the total charge sensing are attenuated.

ΣQR was shown in 2.1.7 to be the no load voltage, which in many processor power supplies is a digital input VID.